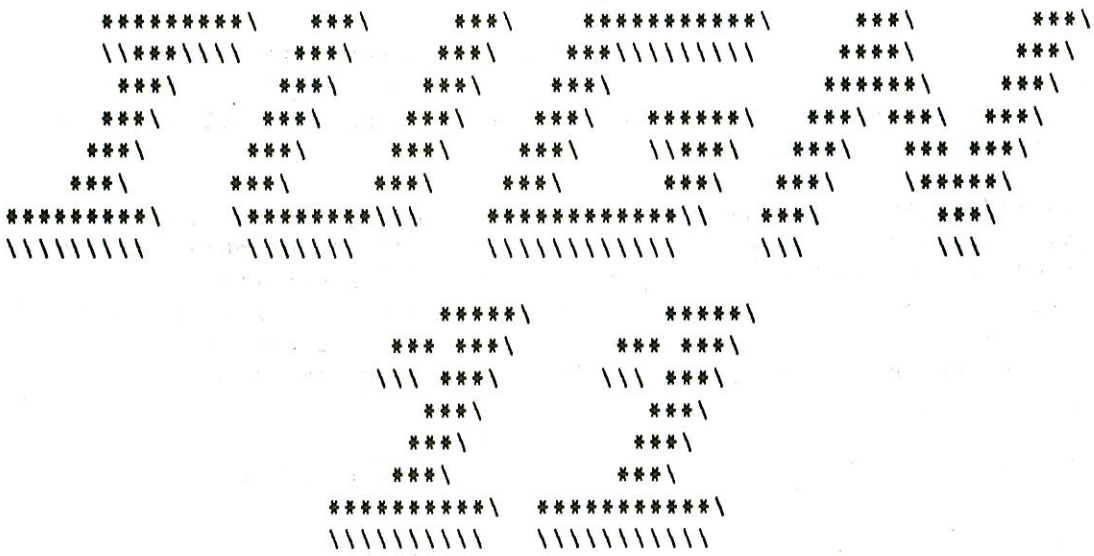
Interaktion

April 1986



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Data Protection Act 1985.
Details of the members of the IUGN are held on computer file. In order to comply with the Data Protection Act, each member may view, alter or destroy any data held on him within that file. To obtain a copy of your own personal file please send a stamped addressed envelope to the Editor. Your subsequent wishes regarding that data will be honoured without question.

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NOTES

CHANGES TO THE USER GROUP ORGANISATION

1. Tom Evans has been elected to the role of Membership Secretary. Please write to him for changes of address and membership. He will also collect and service subscriptions. Hopfully we can publish a set of accounts to show you where the money goes.

2. The software library has been distributed amongst various members. Werever possible the original author has taken over distribution and support of his own product. Where that is not possible one of the committe has assumed responsibility for the program. By this action we hope to give better support and a faster responce to your correspondence. (Don't forget you can still sell your 'gems' through these pages. Just let me know the details for the software index.)

When using ASM 64 and ASM 32 the RLD and RRD instructions must be entered as:-

```
RLD (HL)
RRD (HL)
```

The Mostec numonics RRD and RLD are not accepted by the assembler.

You can now purchase CP/M 2.2 for the Interak direct from Greenbank Electronics. This implimentation can be had on 8", 5.5" and 3.5" drives. The change is very worthwile as it makes the computer a tool, (at last). You need a VDU 2K or a serial terminal plus 20K of RAM to run it. It is probally a good idea to have a chat with Greenbank before you order anything.
I am tempted to start a Public domain disk library. Is there any demand.?

This issue contains a great deal about using the new FDCI floppy disk card and CP/M. For those members who are not interested in this subject I apologise and promise that the summer issue will contain other items. Also this issue contains a lot of stuff written or compiled by me. Other members have submitted some good work which will be in the summer newsletter. I hope you will understand that disks being the new thing for Interak has given rise to a need for the included information. For example the very long work on the 2797 chip is essentual to programming the FDCI card and several members have written requesting that the data be printed. May I suggest to those members who find this issue to be of no use to file it in one of Greenbanks special fancy folders. I lay odds it will be out again within the year.

The October issue was delayed in getting to you because my printer person (David of Greenbank) became ill during the colating process. I know that he regrets the delays and hopes it won't happen again. We are keen to see that the newsletter is good value for money and be on time and whilst there are still problems with the organisation we have the will and in the words of BR "We are getting there".
If you think differently then feel free to write to me. I will publish anything legal.

Bob Eldridge

ADDING SPEECH TO INTERAK

by R.ELDRIDGE

This article presents an implimentation of the SP-0256 speech processor on the Interak computer.

First consider the circuit diagram on the following page.

This should be constructed on a DIP-1 prototyping card with either a built in speaker or a plug to a stereo or power amplifier.

The 74LS,124 provides a variable clock to the speech chip. Adjusting potentiometer VR1 will vary the frequency or pitch of the spoken output.

If it is preferred a crystal can be substituted for the 74LS,124. The crystal should have a value of 3.12MHz and should be connected between pins 27 and 28 on the speech chip.

The 74LS,688 decodes one port of the Z80 I/O interface to provide system access to the speech card. Mapped as follows :-

Port CF "READ" = STATUS, bit 6 (LRQ) if low = send data.
Port CF "WRITE" = DATA to be spoken

The LM324 amplifier provides a filter to the speech output. It shapes this output to improve the sound quality. The filter is not essential and considerable experimentation could be carried out on this part of the circuit. You could for instance take the output directly from the diode (IN4148) to operate without the filter.

The SP-0256 is the speech processor chip. It takes 8 bit data from the computer and outputs an analog signal representing one of 64 phonetic sounds made in human speech. Say to yourself the sound made by the "CH" in "CHURCH" and that is one of the sounds. Another is the "TH" in "THE".

By assembling these sound packages, as a group, virtually all the words in the English language can be spoken. A point to note is that the chip has a slight American accent.

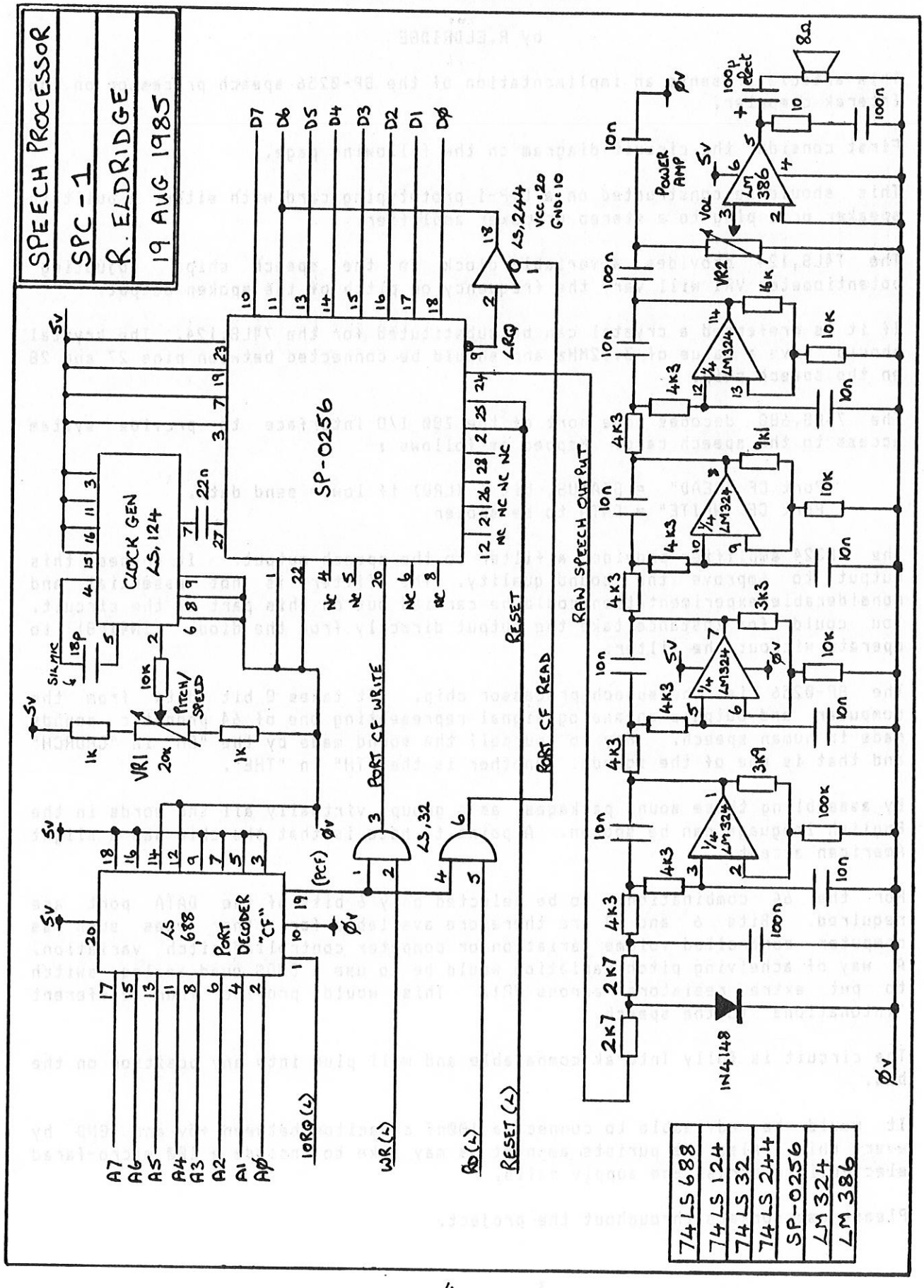
For the 64 combinations to be selected only 6 bits of the DATA port are required. Bits 6 and 7 are therefore available for other uses such as computer controlled volume variation or computer controlled pitch variation. A way of acheiving pitch variation would be to use a CMOS quad analog switch to put extra resistors across VR1. This would provide four different "intonations" to the speech.

The circuit is fully Interak compatable and will plug into any position on the bus.

It would be advisable to connect a 100nf capacitor between +5v and GND by every chip. Also the purists amongst us may like to include a 100 micro-farad electrolitic across the supply rails.

Please use sockets throughout the project.

THE SPEECH PROCESSOR CIRCUIT



The SP-0256 speech processor is an allophonic device which when presented with hex codes 00 through 3F will output a particular speech sound. Words can be constructed by sequentually sending the individual speech sounds that constitute a word, to the chip. I.e :-

To say the word "COMPUTER" send the allophone series :-

KK1-AX-MM-PP1-YY1-UW1-TT2-ER to the chip.

That is send the following data bytes to the chip:-

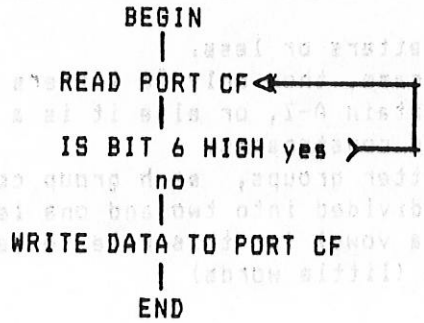
2A, 0F, 10, 09, 31, 16, 0D, 33 to the chip

This particular method of speech construction can be likened to chopping the speech into small pronouceable packets of sound, almost all of the words in the english language can be constructed.

The circuit is port mapped to hex CF. The port is used as follows:-

READ PORT CF --- GET STATUS
WRITE PORT CF --- SEND DATA

The status information consists of one bit, bit 6. This is used to detect LRQ (load register request). When bit 6 goes low a new allophone may be passed to the chip by writing it to port CF.



This mechanism is used in the following basic program to output the phrase :-

"A BIRD IN THE HAND IS WORTH TWO IN THE BUSH"

```
 5 X=40
 7 RESTORE
10 GOSUB 1000
20 READ B
30 OUT (£CF),B
40 X=X-1
50 IF X<>0 GOTO 10
60 STOP
1000 A=IN(£CF)
1020 IF A>=64 GOTO 1000
1030 RETURN
5000 DATA 20,2,63,52,0,21,2,12,11,2,18,19,2,27,26,11
5010 DATA 0,21,3,12,43,2,46,52,29,2,13,31,2,12,11,2
5020 DATA 18,19,2,63,30,37,64,4
```

It is also possible to pass allophones using a machine code driver.

The allophone is passed to the routine in the C register

```
SPEAK:  PUSH AF          ;Stack AF
SPK1:   IN A,(0CFH)      ;Get speech chip status
        BIT 6,A          ;If busy
        JR NZ,SPK1       ;Loop back.  Else...
        LD A,C           ;Get allophone code
        OUT (0CFH),A     ;Give it to speech chip
        POP AF           ;Restore AF
        RET              ;Exit
```

The recomended method for analasis is to read "RAW" text from an input buffer until a full word is detected (punctuation character). Then decode it to an output "PHONE" buffer. Continue doing this until a full sentence has been decoded (Full stop). Then pass the entire phone buffer to the speech chip. Context scanning and vowel/constonant modification can then be performed using the full text of the sentance.

Analasis of the text is normally performed using a series of rules to alter the phones selected. I.e for "DAM" to become "DAME" the "A" sound is altered by the trailing "E".

When considering full text scanning algorithms - words can be :-

Considered to be 15 letters or less.
Converted into upper case, then only 26 letters to scan.
Considered to only contain A-Z, or else it is a non-word.
Broken into vowels and constonants.
Broken into three letter groups, each group containing a vowel, with any remainder divided into two and one letter groups. (Y must be considered a vowel for this rule to be general).
Broken into sillables (little words)

Also :-

Words do not contain non A-Z codes. Any groups that contain non A-Z codes are non-words and are prononced letter by letter. I.e TWC436C

Words without vowels are non-words and should be pronounced letter by letter. I.e BBC

In the following table the "DATA" is what is passed to the chip to cause it to say the "ALLOPHONE". "USEAGE" gives a guide to the sound produced.

DATA	ALLO-PHONE	TIME ms	USEAGE
00	PA1	10	Pause before BB, DD, GG, and JH
01	PA2	30	Pause before BB, DD, GG, and JH
02	PA3	50	Pause before PP, TT, KK, and CH, and between words
03	PA4	100	Pause between clauses and sentences
04	PA5	200	Pause between clauses and sentences
05	OY	290	nOIse, tOY, vOIce
06	AY	170	kIte, skY, mIghty
07	EH	50	Extent, gEntlemen
08	KK3	80	CRane, QUick, Clown, sCream.

09	PP1	150	Pleasure, amPle, triP
0A	JH	100	Judge, inJure
0B	NN1	170	earN
0C	IH	50	sIttIng, strandEd
0D	TT2	100	TesT, sTreeT
0E	RR1	130	Read, WRite, x-Ray
0F	AX	50	lApel, instrUct
10	MM	180	Milk, alarM, aMple
11	TT1	80	tesTs, iTs
12	DH1	140	THis, THen, THey
13	IY	170	trEAt, pEOple, pennY
14	EY	200	grEAt, stAtement, trAY
15	DD1	50	playED, enD
16	UW1	60	comPUter
17	AO	70	tAlking, sOng
18	AA	60	pOttery, cOtton
19	YY2	130	Yes, Yarn, Yo-yo
1A	AE	80	extrAct, Acting
1B	HH1	90	He
1C	BB1	40	fiBBer, Bleed, Brown
1D	TH	130	THin.
1E	UH	70	cOOkie, fUll
1F	UW2	170	tWO, fOOd
20	AW	250	sOUnd, mOUse, dOWn
21	DD2	80	Down, Drain
22	GG3	120	anGer, peG
23	VV	130	Vest, proVe, eVen
24	GG1	80	Guest
25	SH	120	SHirt, leaSH, naTIon
26	ZH	130	beiGE, pleaSure
27	RR2	80	bRown, cRane, gRease
28	FF	110	Food
29	KK2	140	speaK, tasK
2A	KK1	120	Cute, Clown, sCream
2B	ZZ	150	Zoo, phaZe
2C	NG	200	striNG, aNGer
2D	LL	80	Like, heLLo, steeL
2E	WW	140	We, Warrant, linGUist
2F	XR	250	hAIR, declARE, stARE
30	WH	150	WHite, WHim, tWenty
31	YY1	90	cUte, bEAuty, comPUter
32	CH	150	CHurCH, feaTure
33	ER1	110	lettER, fURnitURe, intERrupt
34	ER2	210	bIRd, fERn, bURn
35	OW	170	ZOne, clOse, snOW
36	DH2	180	baTHe, baTHing
37	SS	60	veSt
38	NN2	140	No
39	HH2	130	Hoe
3A	OR	240	fORtune, adORn, stORe
3B	AR	200	fARm, alARm, gARment
3C	YR	250	hEAr, EArring, IRresponsible
3D	GG2	80	Green, Glue
3E	EL	140	littLE, angLE, gentLEmen
3F	BB2	60	Beast

Following are some examples of word constructions :-

Try to read the allophones yourself, this will help you grasp the way words are constructed with them.

WORD	SEND
&	AE,NN1,PA2,DD1
(	OW,PA3,PP1,EH,NN1,PA3,BB1,PA2,RR2,AE,PA3,KK1,EH,PA3,TT2,SS
)	KK3,LL,OW,SS,PA3,BB1,PA2,RR2,AE,PA3,KK1,EH,PA3,TT2,SS
+	PP1,LL,AX,SS
/	SS,SS,PA3,TT2,PA2,RR2,PA3,KK2
0	ZZ,YR,OW,PA3
1	WW,AX,AX,NN1,PA3
2	TT2,UW2,PA3
3	TH,TH,RR1,IY,PA3
4	FF,FF,OR,PA3
5	FF,FF,AY,VV,PA3
6	SS,SS,IH,IH,PA3,KK2,SS,PA3
7	SS,SS,EH,EH,VV,IH,NN1,PA3
8	EY,PA3,TT2,PA3
9	NN1,AA,AY,NN1,PA3
TEN	TT2,EH,EH,NN1
ELEVEN	IH,LL,EH,EH,VV,IH,NN1
TWELVE	TT2,WH,EH,EH,LL,VV
THIRTEEN	TH,ER1,PA2,PA3,TT2,IY,NN1
TWENTY	TT2,WH,EH,EH,NN1,PA2,PA3,TT2,IY
HUNDRED	HH2,AX,AX,NN1,PA2,DD2,RR2,IH,IH,PA1,DD1
THOUSAND	TH,AA,AW,ZZ,IH,PA1,PA1,NN1,DD1
MILLION	MM,IH,IH,LL,YY1,AX,NN1
DAUGHTER	DD2,AO,TT2,ER1
COLLIDE	KK3,AX,LL,AY,DD1
SISTER	SS,SS,IH,SS,TT2,ER1
CLOWN	KK1,LL,AW,NN1
COOKIE	KK3,UH,KK1,IY
LETTER	LL,EH,TT2,ER
LITTLE	LL,IH,TT2,EL
UNCLE	AX,NG,KK3,EL
COMPUTER	KK1,AX,M,PP1,YY1,UW1,TT2,ER
EXTENT	EH,KK1,SS,TT2,EH,EH,NN1,TT2
TWO	TT2,UW2
ALARM	AX,LL,AR,MM
SCORE	SS,KK3,OR
FIR	FF,ER2

THE END

NOTES ON THE 2797 CHIP

COMPILED BY R.ELDRIDGE

These notes are provided in responce to several members requesting information on the 2797 chip as used in the FDCI-1 card. The information has been gleaned from several sources, mostly from the chip data sheets.

279X CHIP FEATURES

* ON-CHIP PLL DATA SEPARATOR
* ON-CHIP WRITE PRECOMPENSATION LOGIC
* SINGLE 5v SUPPLY
* ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS.
 IBM 3740 (FM)
 IBM 34 (MFM)
* AUTOMATIC SEEK WITH VERIFY
* MULTIPLE SECTOR READ/WRITE
* TTL COMPATIBLE
* PROGRAMMABLE CONTROL.
 SELECTABLE TRACK-TO-TRACK ACCESS
 HEAD LOAD TIMING.
* SOFTWARE COMPATIBLE WITH THE FD179X SERIES.
* SOFT SECTOR FORMAT COMPATIBILITY

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Seperator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5.25" or 8" Floppy Disk interfacing.

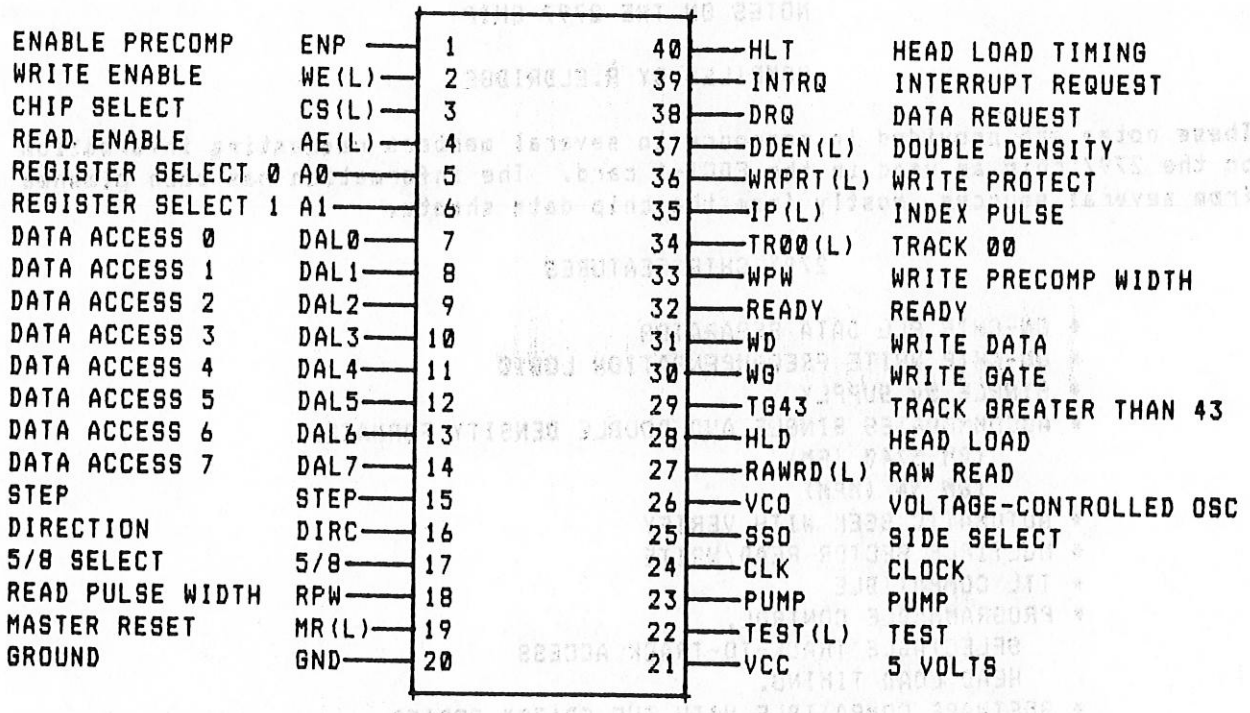
The WD279X is fabricated in NMOS silicon gate technology and is available in a 40 pin dual-in-line ceramic or plastic package.

VARIANTS

FEATURES	2791	2793	2795	2797
SINGLE DENSITY (FM)	X	X	X	X
DOUBLE DENSITY (MFM)	X	X	X	X
TRUE DATA BUS		X		X
INVERTED DATA BUS	X		X	
SIDE SELECT OUT			X	X
INTERNAL CLK DIVIDE	X	X		

The Interak FDCI-1 card is designed around the 2797 version of the chip.

The notes that follow pertain primarally to the 2797 version.



1 ENP..... ENABLE PRECOMP ------ A logic high on this input enables write precompensation to be performed on the Write Data output.

2 WE(L)... WRITE ENABLE -------- A logic low on this input gates data on the DAL into the selected register when CS(L) is low.

3 CS(L)... CHIP SELECT --------- A logic low on this input selects the chip and enables computer communication with the device.

4 AE(L)... READ ENABLE --------- A logic low on this input controls the placement of data from a selected register on the DAL when CS(L) is low.

5 A0..... REGISTER SELECT 0 --- These two inputs select the register to
6 A1..... REGISTER SELECT 1 receive/transfer data on the DAL lines under RE(L) and WE(L) control.

CS(L)	A1	A0	RE(L)	WE(L)
0	0	0	Status reg	Command reg
0	0	1	Track reg	Track reg
0	1	0	Sector reg	Sector reg
0	1	1	Data reg	Data reg

7 DAL0.... DATA ACCESS 0 ------- Eight bit bi-directional bus used for
8 DAL1.... DATA ACCESS 1 transfer of commands, status, and data.
9 DAL2.... DATA ACCESS 2 These lines are inverted (active low) on
10 DAL3.... DATA ACCESS 3 2791 & 2795 chips.
11 DAL4.... DATA ACCESS 4 True (active high) on 2793 and INTERAKS
12 DAL5.... DATA ACCESS 5 2797 chip.
13 DAL6.... DATA ACCESS 6
14 DAL7.... DATA ACCESS 7

15 STEP.... STEP ---------- This output is a pulse for each step.

16 DIRC.... DIRECTION ---------- Direction output is high when stepping in, low when stepping out.

17 5/8..... 5/8 SELECT ---------- This input selects the internal VCO frequency for use with 5.25" drives or 8" drives. 5.25" Low, 8" High.

18 RPW..... READ PULSE WIDTH ---- An external potentiometer tied to this input controls a phase comparator within the data separator.

19 MR(L)... MASTER RESET -------- A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status bit 7) is reset during MR ACTIVE. When MR(L) is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register.

20 GND..... GROUND ---------- Connect to ground or zero volts.

21 VCC..... 5 VOLTS ---------- Connect to 5v +- 5%

22 TEST(L). TEST ---------- A logic low on this input allows adjustment of external resistors by enabling internal signals to apppear on selected pins.

23 PUMP ... PUMP ---------- High impedance output signal which is forced high or low to increase or decrease VCO frequency.

24 CLK CLOCK ---------- This input requires a free running 50% duty cycle square wave clock for internal timing reference. 2 MHz for 8" drives, 1MHz for 5.25" drives.

25 SSO SIDE SELECT --------- 2795,2797 chips only. The logic level of the Side Select Output is directly controlled by the 'S' flag in Type 2 or 3 commands. When U= 1, SSO is set to a logic 1. When U= 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector ID field If they do not compare Status bit 4 (RNF) is set. The side select output is only updated at the beginning of a type 2 or 3 command. It is forced to a logic 0 upon a MASTER RESET condition.

26 VCO VOLTAGE-CONTROLED OSC An external capacitor tied to this pin adjusts the VCO center frequency.

27 RAWRD(L) RAW READ ---------- The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.

28 HLD HEAD LOAD ---------- The HLD output controls the loading of the head against the media.

29 TG43 ... TRACK GREATER THAN 43 This output informs the drive that the head is positioned between tracks 44-76. This output is valid only during Read/Write commands.

30 WG WRITE GATE ---------- This output is made valid before writing is to be performed on the diskette.

31 WD WRITE DATA ---------- A 250ns (MFM) or 500ns (FM) output pulse per flux transition. WD contains the unigue Address marks as well as data and clock in both FM and MFM formats.

32 READY .. READY --------------- This input indicates disk readiness and is sampled for a high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an INTRQ is generated. Type 1 operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status bit 7.

33 WPW WRITE PRECOMP WIDTH - An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.

34 TR00(L). TRACK 00 ------------ This input informs the WD2797 that the head is positioned over track 0.

35 IP(L) .. INDEX PULSE --------- This input informs the WD2797 when the index hole is encountered on the diskette.

36 WRPRT(L) WRITE PROTECT ------- This input is sampled whenever a Write Command is received. A low terminates the command and sets the "Write Protect" Status Bit.

37 DDEN(L). DOUBLE DENSITY ------ This input pin selects either single or double density operation.
DDEN = 0, double density is selected.
DDEN = 1, single density is selected.

38 DRQ DATA REQUEST -------- This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.

39 INTRQ .. INTERRUPT REQUEST --- This output is set at the completion of any command and is reset when the Status register is read from or the command register is written to.

40 HLT HEAD LOAD TIMING ---- When a high is found on the HLT input the head is assumed to be engaged. It is typically derived from a one-shot triggered by HLD.

GENERAL DESCRIPTION

The WD2797 are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implimentation.

The 2797 is IBM compatible in single density mode (FM) and and system 34 compatible in Double Density Mode (MFM).

The 2797 contains all the features of its predecessor the 179x plus a high performance Phase-Lock-Loop Data Separator as well as Write precompensation logic.

In Double Density mode, Write precompensation is automatically engaged to a value programmed via an external potentiometer.

The processor interface consists of an 8 bit bi-directional bus for data, status and control byte transfers. The 2797 is set up to operate on a multiplexed bus with other bus oriented devices.

The 2797 is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads.

The 2795/2797 package has a side select output for controlling double sided drives.

CHIP ORGANIZATION

INTERAK 1 FDCI-1 PORT MAP

PORT	READ	WRITE
80	STATUS REGISTER	COMMAND REGISTER
81	TRACK REGISTER	TRACK REGISTER
82	SECTOR REGISTER	SECTOR REGISTER
83	DATA REGISTER	DATA REGISTER
84	DISK POLL	not used
85	DISK CONFIG READ	DISK CONFIG WRITE
86	DISK OPTIONS	not used
87	not used	not used

STATUS REGISTER (INTERAK PORT READ 80)
This 8 bit register holds device Status Information. The meaning of the Status bits is a function of the type of command previosly executed. This register can be read onto the DAL, but not loaded from the DAL.

COMMAND REGISTER (INTERAK PORT WRITE 80)
This 8 bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force INTRQ. The command register can be loaded from the DAL, but not read onto the DAL.

TRACK REGISTER (INTERAK PORT READ/WRITE 81)
This 8 bit register holds the track number of the current head position. It is incremented by one every time the head is stepped in, and decremented by one when the head is stepped out. The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

SECTOR REGISTER (INTERAK PORT READ/WRITE 82)
This 8 bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the

ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

DATA REGISTER (INTERAK PORT READ/WRITE 83)
This 8 bit register is used as a holding register during Disk Read and Write operations. In disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.
When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

DATA SHIFT REGISTER
This 8 bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output (WRITE DATA) during write operations.

CRC LOGIC
This logic is used to check or to generate the 16 bit Cyclic Redundancy Check (CRC). The polynomial is G(x) = X^16 + X^12 + X^5 + 1
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC Register is preset to all ones prior to data being shifted through the circuit.

ARITHMETIC LOGIC UNIT
The ALU is a serial comparitor, incrementor and decrementor. It is used for register modification and comparisons with the disk recorded ID field.

TIMING AND CONTROL
All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM DETECTOR
The address mark detector detects ID, data and index address marks during read and write operations.

WRITE PRECOMPENSATION
Enables write precompensation to be performed on the Write Data output.

DATA SEPARATOR
A high performance Phase-Lock-Loop Data Separator with on chip VCO and phase comparator allows adjustable frequency range for 5.25" or 8" Floppy Disk Interfacing.

THE PROCESSOR INTERFACE

The Interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status and Control words out of, or in to the 2797. The DAL are tri-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are low. Or they act as input receivers when CS and Write Enable (WE) are low.

When transfer of data with the 2797 is required by the host computer, the device address is decoded and CS goes low. The address bits A1 and A0 combine with the signals RE, during Read, or WE, during Write to select the following registers :-

CS	A1	A0	read RE	write WE
0	0	0	Status reg	Command reg
0	0	1	Track reg	Track reg
0	1	0	Sector reg	Sector reg
0	1	1	Data reg	Data reg

During Direct Memory Access (DMA) types of data transfers between the Data Register and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the DRQ is set when an assembled serial input byte is transferred to the Data Register. This bit is reset when the Data Register is read by the processor. If the Data Register is read after one or more bytes are lost, by having new data transferred into the Data Register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On disk Write operations the DRQ bit is set when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command is met.

The 2797 has two modes of operation according to the state of DDEN .

DDEN = 1 = Single density (FM)
DDEN = 0 = Double density (MFM)

In either case the CLK input is set at 2MHz for 8" drives or 1MHz for 5.25" drives.

FUNCTIONAL DESCRIPTION

The 2797 is software compatible with the 179x series of disk controllers. Software generated for the 179x can be transferred to a 2797 system without modification.

In addition to the 179x, the 2797 contains an internal Data Separator and Write precompensation circuit. The TEST line is used to adjust both data separator and precompensation.

When TEST = 0 the WD line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW line can then be accomplished. A

second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly Data separation is also adjusted with TEST = 0. The TG43 line is internally connected to the output of the read data one-shot, which is adjusted via the RPW line. The DIRC line contains the read clock signal, (0.5 Mhz for 8" drives). The VCO trimming capacitor is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit.

The TEST(L) line also contains a pull-up resistor so adjustments can be performed simply by grounding the TEST pin, overriding the pull-up. The TEST pin cannot be used to disable stepping rates during operation as its function is quite different from the 179x.

Other pins on the device also include pull-up resistors and may be left open to satisfy a logic one condition :- ENP, 5/8, ENMF, WPRT, DDEN

GENERAL DISK READ OPERATIONS

Sector lengths are determined at format time by the fourth byte in the ID field and bit 3 in type 2 commands I.e

BIT 3 IN TYPE 2 COMMANDS (L) (READ SECTOR) (WRITE SECTOR)	SECTOR LENGTH FIELD (HEX) FOURTH BYTE IN ID FIELD	NUMBER OF BYTES IN SECTOR (DECIMAL)
0	03	128
1	00	128
0	00	256
1	01	256
0	01	512
1	02	512
0	02	1024
1	03	1024

The number of sectors/track as far as the 2797 is concerned is 1-255.
The number of tracks as far as the 2797 is concerned is 0-255.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register (DR) in response to a Data Request from the 2797 before WG can be activated.

Writing is inhibited when the Write Protect input is low. In which case any Write command is immediatly terminated, an INTRQ is generated and the Write Protect bit set. (Status bit 6).

For write operations, the 2797 provides Write Gate and Write Data outputs. Write data consists of a series of pulses set to a width of approximately three times greater than the precomp adjustment.
Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type 2 or 3) is recived the 2797 samples the Ready input. If this is low the command is not executed and an INTRQ is generated.

All type 1 commands are performed regardless of the state of the Ready input.

Whenever a type 2 or 3 command is received, the TG43 line is updated.

TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The 2797 will accept eleven commands.

Command bytes should be loaded into the Command Register when the Busy Status bit is low. The one exception to this is the Force Interrupt command.

Whenever a command is being executed, the Busy status bit is set.

When a command is completed, an INTRQ is generated and Busy is reset.
The Status register indicates wether the completed command encountered an error or was fault free.

For ease of discussion, commands are divided into four types. These are summarized overleaf :-

COMMAND SUMMARY FOR 2797 CHIP

TYPE	COMMAND	7	6	5	4	3	2	1	0
1	RESTORE	0	0	0	0	H	V	R1	R0
1	SEEK	0	0	0	1	H	V	R1	R0
1	STEP	0	0	1	T	H	V	R1	R0
1	STEP-IN	0	1	0	T	H	V	R1	R0
1	STEP-OUT	0	1	1	T	H	V	R1	R0
2	READ SECTOR	1	0	0	M	L	E	U	0
2	WRITE SECTOR	1	0	1	M	L	E	U	A0
3	READ ADDRESS	1	1	0	0	0	E	U	0
3	READ TRACK	1	1	1	0	0	E	U	0
3	WRITE TRACK	1	1	1	1	0	E	U	0
4	FORCE INTERRUPT	1	1	0	1	I3	I2	I1	I0

BITS

T is Track update flag
T = 0 Do not update
T = 1 Update track register

H is Head load flag
H = 0 Unload head at begining
H = 1 Load head at begining

V is Verify track number
V = 0 Do not verify
V = 1 Verify on destination track

R1,R0 are Stepping motor rate

R1	R0	CLK= 2MHz	CLK= 1MHz
0	0	3ms	6ms
0	1	6ms	12ms
1	0	10ms	20ms
1	1	15ms	30ms

A0 is Data address mark
A0 = 0 FB (DAM)
A0 = 1 F8 (deleted DAM)

M is Multiple record flag
M = 0 Single records
M = 1 Multiple records

L is Sector length flag
LSB's of Sector length in ID field

	00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

E is 15ms delay
E = 0 No 15ms delay
E = 1 15 ms delay (30ms for 1MHz)

U is Update Side Select output
U = 0 Update SSO to 0
U = 1 Update SSO to 1

Ix is Interrupt condition flags i.e. produce INTRQ
I0 = 1 Not ready to Ready transition
I1 = 1 Ready to not Ready transition
I2 = 1 Index pulse
I3 = 1 Immediate interrupt, requires a reset
I3-I0 = 0 Terminate with no interrupt, (INTRQ)

WRITE PRE-COMPENSATION - ADJUSTING WRITE PRECOMP SIGNAL (10K POT)
When operating in Double Density mode (DDEN= 0), the 2797 has the capacity of providing a user defined precompensation value for Write Data. An external pot (10K) tied to the WPW signal allows a setting of 100n to 300ns from nominal.

Setting the Write precomp value is accomplished by forcing the TEST pin to 0. A stream of pulses can then be seen on the Write Data line (WD). Adjust the WPW pot for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (WG) is inactive while TEST= 0.

DATA SEPARATION
The 2797 can operate with either an external data separator or its own internal recovery circuits. The condition of the TEST line in conjuction with MR will select internal or external mode.

ADJUSTING READ DATA PULSE (50K POT) AND CENTER FREQUENCY (TRIM CAP)
To adjust the internal VCO operation (used by Interak FDCI-1), the TEST line must be high during the MR pulse, then set low for the adjustment procedure.

A 50K pot tied to the RPW input is used to set the internal Read Data pulse for proper phasing. With a scope on TG43, adjust the RPW pulse for 1/8 of the data rate (250ns = 8" double density). An external variable capacitor of 5-60pf is tied to the VCO input for adjusting center frequency. With a scope on DIRC adjust the trimmer cap to yield the required data rate (500KHz for 8" double density). The DDEN line must be low while the 5/8 line is held high or the adjustment times will be doubled.

After adjustments have been made, the TEST pin is returned to a logic high and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output. This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the responce to normal frequency shift i.e, the lock-up time. A balance must first be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremley wide lock-up response, leading to PUMP run-away. The fillter affects these two reactions in mutually opposite directions.

The source impedence for a PUMP-UP/PUMP-DOWN condition is 600/120 ohms, respectivly therefore the change in bias voltage for each pump can be approximated to :-

$$dV = \frac{dt\ deltaV}{RC}$$

dt = 250ns (set by RPW)
C = 0.1 microfarads
R = Rs + R
deltaV = 2.6V for PUMP UP
0.9V for PUMP DOWN

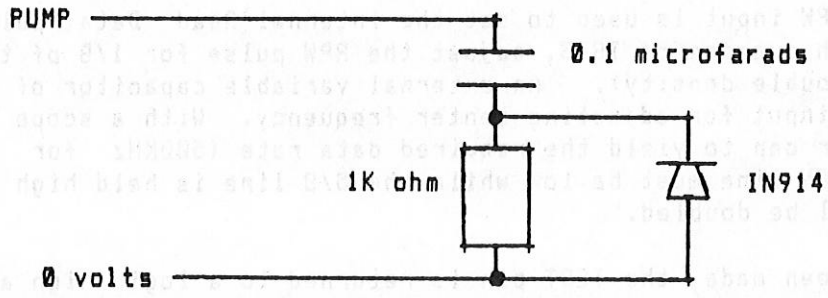
Lock up responce (TL) is the transient time for the loop to lock from center frequency (F0) to maximum lock range.

TL = 10% FL * K0 * deltaP

Where :- K0 = VCO conversion gain = 3.7KHz/mV
FL = Lock range = 4MHz
deltaP = Change in bias for each pump = 4mV/PUMP

400KHz * 3.7KHz * 4mV = 27 pumps
27 pumps = 54 microsecs = 3.4 byte times (8" double density)

The following filter circuit is recommended for 8" FM/MFM :-



Since 5.25" drives operate at exactly one-half the data rate (250Kb/sec) the above capacitor should be doubled to 0.2 microfarads or 0.22 microfarads. (Interak FDCI uses quad analog switch to effect this).

TYPE 1 COMMANDS

The type 1 commands include :- Restore, Seek, Step, Step-in, Step-out. Each of the type 1 commands contain a rate field (R1, R0), which determines the stepping motor rate.

R1	R0	CLK= 2MHz	CLK= 1MHz
0	0	3ms	6ms
0	1	6ms	12ms
1	0	10ms	20ms
0	1	15ms	30ms

A 2 microsec (MFM) or 4 microsec (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in the direction determined by the DIRC output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The DIRC signal is high when stepping in and low when stepping out. The DIRC signal is valid 12 microsecs before the first stepping pulse is generated.

After the last directional step an additional 15 millsecs of head settling time takes place if the Verify flag = 1 in type 1 commands. Note that this

time doubles to 30 millisecs for a 1MHz clock. There is also a 15ms head settling time if the E flag is set in any type 2 or 3 command.

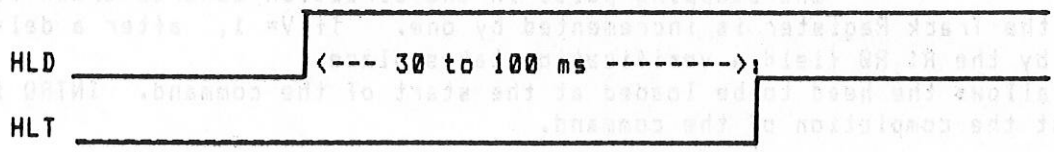
When a Seek, Step or Restore command is executed an optional verification of head position can be performed by setting bit 2 (The V bit) in the command byte. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register. If the track numbers compare and the ID field CRC is correct the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set, and the next encountered ID field is read for the verification operation.

The 2797 must find an ID field with correct track number and correct CRC within 5 revolutions of the disk; otherwise the seek error bit is set and an INTRQ is generated. If V= 0, no verification is performed.

The Head Load (HLD) output controls the movement of the head against the media. HLD is activated at the begining of a type 1 command if the H flag is set, or at the end of the type 1 command if V= 1, or upon receipt of any type 2 or 3 command. Once HLD is active it remains active untill either a type 1 command is received with H= 0 and V= 0; or if the 2797 is in an idle state and 15 index pulses have occured.

Head Load (HLD) is an input to the 2797 which is used for the head engage time. When HLT= 1, the 2797 assumes the head is completley engaged. The head engage time is typically 30 to 100ms depending on the drive type. The low to high transition on HLD is typically used to fire a one-shot. The output of the one-shot is then used for HLT and returned as an input to the 2797.

HEAD LOAD TIMING



When both HLD and HLT are true, the 2797 will read or write to the disk. The "and" of HLD and HLT apears as status bit 5 in type 1 status.

SUMMARY OF H & V FLAGS FOR TYPE 1 COMMANDS

H	V	HLD
0	0	Reset
1	0	Set at the beginning of the command and HLT is not sampled nor is there an internal 15ms delay.
0	1	Set near the end of the command, an internal 15ms delay occurs and the 2797 waits for HLT to be true.
1	1	Set at the beginning of the command. Near the end of the command, after all the steps have been issued, a 15ms delay occurs and the 2797 waits for HLT

For all type 2 and 3 commands with E = 0, HLD is set and HLT is sampled until true. With E= 1, HLD is set, an internal 15ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0) COMMAND -------- Upon receipt of this command the Track 00 (TR00) input is sampled. If TR00 = 0, indicating the head is over track 0, the Track Register is loaded with 00 and an INTRQ is generated. If TR00 = 1, stepping pulses at a rate specified by the R1,R0 field are issued until TR00 = 0. At this time the Track Register is loaded with 00 and INTRQ is generated. If TR00 does not go low after 255 stepping pulses, the 2797 terminates the command, sets INTRQ, and sets the Seek Error status bit. If V= 1 a verification operation takes place. The H bit allows the head to be loaded at the start of the command. Note that the Restore command is executed when MR goes from 0 to 1.

SEEK COMMAND -------- This command assumes that the Track Register contains the track number of the current position of the head and the Data Register contains the desired track number. The 2797 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register. If V= 1 a verification operation takes place. The H flag allows the head to be loaded at the start of the command. INTRQ is generated at the completion of the command. Note: When using multiple drives, the Track Register must be updated for the drive selected before Seeks are issued.

STEP COMMAND -------- Upon receipt of this command, the 2797 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the R1,R0 field,a verification takes place if V = 1.
If T = 1, the Track Register is updated. The H flag allows the head to be loaded at the start of the command. INTRQ is generated at the completion of the command.

STEP-IN COMMAND -------- Upon receipt of this command, the 2797 issues one stepping pulse in the direction towards track 76.
If T = 1, the Track Register is incremented by one. If V= 1, after a delay determined by the R1,R0 field,a verification takes place.
The H flag allows the head to be loaded at the start of the command. INTRQ is generated at the completion of the command.

STEP-OUT COMMAND -------- Upon receipt of this command, the 2797 issues one stepping pulse in the direction towards track 0.
If T = 1, the Track Register is decremented by one. If V= 1, after a delay determined by the R1,R0 field,a verification takes place.
The H flag allows the head to be loaded at the start of the command. INTRQ is generated at the completion of the command.

EXCEPTIONS
On the 2797, the SSO output is not affected during type 1 commands, and an internal side compare does not take place when V = 1.

TYPE 2 COMMANDS

The type 2 commands are the Read Sector and Write Sector commands. Prior to loading the type 2 command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the type 2 command, the BUSY status bit is set. If E= 1 (this is the normal case) HLD is set to 1 and HLT is sampled after a 15ms delay. If E= 0 the head is loaded

and HLT sampled with no 15ms delay.

When an ID field is located on the disk, the 2797 compares the track number on the ID field with the Track Register. If there is no match the next encountered ID field is read and a comparison made again. If there was a match, the sector number of the ID field is compared with the Sector Register. If there is no sector match the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from, depending upon the command. The 2797 must find an ID field with a track number, sector number, side number, and CRC within 5 revolutions of the disk; otherwise the Record Not Found status bit is set and the command is terminated with INTRQ.

Each of the type 2 commands contains an M flag which determins if multiple records (sectors) are to be read or written, depending upon the command. If M = 0, a single sector is accessed and INTRQ is generated at the completion of the command. If M = 1, multiple sectors are accessed with the Sector Register internally updated so that verification can occur on the next sector. The 2797 will continue to read/write multiple sectors and update the Sectot Register in numerical ascending sequence untill the Sector Register exceeds the number of sectors on the track or untill the Force Interrupt command is loaded into the Command Register, which terminates the command and generates INTRQ.

For example: If the 2797 is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The 2797 will search for 5 disk revolutions, INTRQ out, reset busy, and set record not found in the status byte.

The type 2 and type 3 commands contain a side select flag U.
When U = 0, SSO is reset to 0.
When U = 1, SSO is set to 1.
The chip compares the SSO to the ID field. If they do not compare within 5 revolutions INTRQ is generated and RNF (record not found) set in the status byte.

The Read Sector and Write Sector commands include a "L" flag. The "L" flag, in conjunction with the sector length byte of the ID field, allows different byte counts to be implimented in each sector. For IBM compatibility , L should be set to one.

READ SECTOR COMMAND -------- Upon receipt of the Read Sector command, the head is loaded, the busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes, in single density, and 43 bytes in double density, of the last ID field CRC byte; if not, search of the ID field is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data status bit is set. This sequence continues untill the complete data field has

been inputted to the computer. If there is a CRC error, at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).
At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register bit 5 as :-

STATUS BIT 5	TYPE OF DATA MARK ENCOUNTERED
0	Deleted Data Mark (DAM)
1	Data Mark (DM)

WRITE SECTOR COMMAND -------- Upon receipt of the Write Sector command, the head is loaded, the busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 2797 counts off 11 bytes in single density, and 22 bytes in double density from the CRC field and the WG output is activated. If the DRQ is serviced (I.e. the DR has been loaded by the computer), (If DRQ has not been serviced, the command is terminated and Lost Data status set). If the DRQ has been serviced, the WG is made active and 6 bytes of zeroes in single density, and 12 bytes in double density, are written to the disk. At this time the Data Address Mark is written as determined by the A0 flag of the command as shown below :-

A0	DATA ADDRESS MARK
0	Deleted Data Mark
1	Data Mark

The 2797 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data status bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two byte CRC is computed internally and written on the disk followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2MHz clock the INTRQ will set 8 to 12 microseconds after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the Lost Data status and improper CRC bytes.

TYPE 3 COMMANDS

READ ADDRESS COMMAND -------- Upon receipt of the Read Address command, the head is loaded and the Busy Status bit is set. The next encountered ID field is then read from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below :-

BYTE No =	1	2	3	4	5	6
	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2

Although the CRC characters are transferred to the computer, the 2797 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the Sector Register so that a comparison can be made by the computer. At the end of the operation an INTRQ is generated and the Busy status bit is reset.

READ TRACK COMMAND -------- Upon receipt of the Read Track command, the head is loaded, and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and Data bytes are assembled and transferred to the Data Register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An INTRQ is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are :-

No CRC checking is performed.
Gap information is included in the data stream.
The internal side compare is not performed.
The address mark detector is on for the duration of the command.

Because the AM detector is always on, write splices or noise may cause the chip to look for an AM. If an address mark does not appear on schedule the Lost Data flag is set.

The ID A.M, ID field, ID CRC bytes, DAM, Data and Data CRC bytes for each sector will be correct. The Gap bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

Formatting the disk is a relatively simple task when operating with a large amount of memory. Data and Gap information must be provided to the 2797 chip. Formatting the disk is accomplished by positioning the head over the desired track and issuing a Write Track command.

WRITE TRACK COMMAND -------- Upon receipt of the Write track command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered Index pulse and continues until the next Index pulse, at which time INTRQ is activated. DRQ is activated imediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the Index pulse is encountered the operation is terminated, Lost Data is set in the status byte and INTRQ is generated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk. However, if the 2797 detects a byte of F5 through FE in the DR, the data written to the disk will not be the contents of the DR. The 2797 will interpret those bytes so as to produce, say Data Address Marks or a CRC generation.

CONTROL BYTES FOR INITIALIZATION

DATA	INTERPRETATION IN FM, DDEN=1	INTERPRETATION IN MFM, DDEN=0
00-F4	write 00-F4 with CLK = FF	write 00-F4, in MFM
F5	not allowed	write A1* in MFM, preset CRC
F6	not allowed	write C2** in MFM
F7	generate 2 CRC bytes	generate 2 CRC bytes
F8-FB	write F8-FB,CLK=C7,preset CRC	write F8-FB, in MFM
FC	write FC with CLK = D7	write FC in MFM
FD	write FD with CLK = FF	write FD in MFM
FE	write FE,CLK = C7, preset CRC	write FE in MFM
FF	write FF with CLK = FF	write FF in MFM

* = Missing clock transition between bits 4 and 5.
** = Missing clock transition between bits 3 and 4.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. As a consequence, the bytes F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 byte.

TYPE 5 COMMANDS

FORCED INTERRUPT COMMAND -------- The Forced Interrupt command is generally used to terminate a multiple sector read/write command or to insure type 1 status is in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy set) the command will be terminated and the Busy bit reset.
The four lower bits of the command byte determine the conditional INTRQ as follows :-

I0 = Not-Ready to Ready Transition
I1 = Ready to Not-Ready Transition
I2 = Every Index Pulse
I3 = Immediate INTRQ

The conditional INTRQ is enabled when the corresponding bit positions of the command, (I3,I2,I1,I0), are set to 1. Then, when the condition is met INTRQ will go high signifying that the condition specified has occured. If I3,I2,I1,I0 are all set to 0 (HEX D0), no INTRQ will occur but any command presently under execution will be immediately terminated. When using the immediate INTRQ condition (I3=1), (HEX D8), an INTRQ will be immediately generated and the current command terminated. Reading the status or writing to the Command Register will not automatically clear the INTRQ. The HEX D0 is the only command that will enable the immediate INTRQ (HEX D8) to clear on a subsequent load Command Register or Read Status Register operation. Follow a HEX D8 command with a HEX D0 command.

Wait 8 microseconds (double density) or 16 microseconds (single density) before issuing a new command after issuing a Forced Interrupt (times double when clock = 1MHz). Loading a new command sooner than this will nullify the Forced Interrupt.

Forced Interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced Interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc).

More than one condition may be set at a time. If for example, the Ready to Not-Ready condition (I1) and the Every Index Pulse condition (I2) are set, the resultant command would be HEX DA. The "OR" function is performed so that either condition will cause an INTRQ.

STATUS REGISTER

Upon receipt of any command except the Force Interrupt command, the Busy bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt command is received when there is a current command under execution, the Busy bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the busy bit is reset and the rest of the status bits are cleared or updated. In this case, Status reflects the type 1 commands.

When the Data Register is read the DRQ bit in the Status Register and the DRQ line are reset. A write to the Data Register also causes both DRQ's to be reset.

The Busy bit in the Status Register may be monitored with a program to determine when a command is complete, in lieu of using the INTRQ line. When using INTRQ, a busy status check is not recommended because a read of the Status Register to determine the condition of busy will reset the INTRQ line.

Because of internal sync cycles, certain time delays must be observed when operating under progammed I/O. They are :-

OPERATION	NEXT OPERATION	DELAY REQ'D* FM	MFM
Write to Command Reg	Read Busy bit (Status bit 0)	12	6
Write to Command Reg	Read Status bits 1-7	28	14
Write any Register	Read from a different register	0	0

* =Delay required in microseconds

The layout of the Status byte is as follows :-

BIT =	7	6	5	4	3	2	1	0
	S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed :-

STATUS REGISTER SUMMARY

BIT	TYPE 1 COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS DECODE FOR TYPE 1 COMMANDS

BIT NAME	STATE	MEANING
S7 NOT READY	0 1	Drive is Ready. Commands obeyed Drive is Not Ready Commands obeyed
S6 PROTECTED	0 1	Not Write protected Write protected
S5 HEAD LOADED	0 1	Head is not loaded Head is loaded
S4 SEEK ERROR	0 1	Reset to 0 when updated Desired track not verified
S3 CRC ERROR	0 1	Reset to 0 when updated CRC error
S2 TRACK 00	0 1	Not at track 00 Head is over track 00
S1 INDEX	0 1	Index mark detected
S0 BUSY	0 1	No command in progress Command in progress

STATUS DECODE FOR TYPE 2 AND TYPE 3 COMMANDS

BIT NAME	STATE	MEANING
S7 NOT READY	0 1	Drive is Ready Commands obeyed Drive is Not Ready. Commands ignored
S6 PROTECTED	0 1	Reset when updated. Write protected
S5 RECORD TYPE	0 1	On Read record = Data Mark On Read record = Deleted Data Mark
S4 RECORD NOT FOUND (RNF)	0 1	Reset when updated. Desired track,sector, or side not found.
S3 CRC ERROR	0 1	Reset when updated CRC error (S4=1= ID error else DATA error)
S2 LOST DATA	0 1	Reset when updated. Did not respond to DRQ in one byte time.
S1 DATA REQUEST (DRQ)	0 1	Reset when updated On Read DR is full, On Write DR is empty.
S0 BUSY	0 1	No command in progress Command in progress

SUMMARY OF ADJUSTMENT PROCEDURE FOR 2797 CHIP

WRITE PRECOMPENSATION

1) Set TEST (pin 22) to a logic high.
2) Pulse MR (pin 19) low. (Reset).
3) Set TEST (pin 22) to a logic low.
4) Observe pulse width on WD (pin 31)
5) Adjust WPW (pin 33) for desired pulse width (precomp value).
6) Set TEST (pin 22) to a logic high.

DATA SEPARATOR

1) Set TEST (pin 22) to a logic high.
2) Pulse MR (pin 19 low. (Reset).
3) Set TEST (pin 22) to a logic low.
4) Observe pulse width on TG43 (pin 29).
5) Adjust RPW (pin 18) for 1/8 of read clock.
 (250ns for 8" DD, 500ns for 5.25"DD, etc)
6) Observe frequency on DIRC (pin 16)
7) Adjust variable capacitor on VCO pin for data rate.
 (500KHz for 8" DD, 250KHz for 5.25"DD, etc).
8) Set TEST (pin 22) to a logic high.

Note: To maintain internal VCO operation, insure that TEST=1 whenever a Master Reset (MR) pulse is applied.

DISK FORMATTING
Shown below is the IBM single-density format with 128 bytes/sector.

In order to format a diskette, the user must issue a Write Track command, and load the Data Register with the following values.

For every byte to be written, there is one DRQ. :-

NUMBER OF BYTES (DECIMAL)	HEX VALUE OF DATA OR DESCRIPTION OF DATA TO WRITE	
40	FF or 00	
6	00	
1	FC Index Mark	
26	FF or 00	
6	00	WRITE THIS FIELD 26 TIMES. (SECTOR DATA)
1	FE ID Address Mark	
1	-- Track Number 00 - 4C	
1	-- Side Number 00 or 01	
1	-- Sector Number 01 - 1A	
1	00 Sector Length	
1	F7 Writes 2 CRC bytes	
11	FF or 00	
6	00	
1	FB Data Address Mark	
128	-- Data IBM uses E5	
1	F7 Writes 2 CRC bytes	
27	FF	

After 26 sectors have been written, continue writing till 2797 raises INTRQ. Approx 247 bytes.

Shown overleaf is the IBM double-density format with 256 bytes/sector. In order to format a diskette, the user must issue a Write Track command, and load the Data Register with the following values. For every byte to be written, there is one DRQ. :-

NUMBER OF BYTES (DECIMAL)	HEX VALUE OF DATA OR DESCRIPTION OF DATA TO WRITE	
80	4E	
12	00	
3	F6 Writes C2	
1	FC Index Mark	
50	4E	
12	00	←
3	F5 Writes A1	
1	FE ID Address Mark	
1	__ Track Number 00 - 4C	
1	__ Side Number 00 or 01	
1	__ Sector Number 01 - 1A	WRITE THIS
1	01 Sector Length	FIELD 26
1	F7 Writes 2 CRC bytes	TIMES.
22	4E	
12	00	(SECTOR DATA)
3	F5 Writes A1	
1	FB Data Address Mark	
256	__ Data IBM uses E5	
1	F7 Writes 2 CRC bytes	
54	4E	←

After 26 sectors have been written, continue writing till 2797 raises INTRQ. Approx 598 bytes.

NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met :-

1) Sector size must be 128, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 2797. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 2797 operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achive proper operation.

It is recommended that the IBM format be used for highest system reliability.

More information on formatting will be published in later issues.

The INTERAK 1 standard format is listed elsware in this issue.

AN EXAMPLE USING THE FDCI CARD

To understand how to use the 2797 chip and the FDCI card I have written a skeleton BOOT routine for you to study.

This executes at E000 and reads the first 512 byte sector from track 0 into store at C000. It then moves the first 128 bytes of the data to store location 80. Finally passing control to the code at 80.

The routine is typical of a CP/M boot routine. I.e. To boot CP/M :-

1 Read 128 bytes from sector 1 track 0 to address 80.
2 Execute the code at 80.
3 The code at 80 reads in CP/M from tracks 1 and Ø, loading the code to the CP/M destination address.
4 Execute the CP/M code.

The following routine performs step 1. (THE BOOT)

```
E000                    ORG 0E000H      ;Boot rom start address

E000  31FFDF BOOT:      LD SP,0DFFFH    ;Load stack pointer
E003  DBFF              IN A,(0FFH)     ;Switch off power jump
E005  3E40              LD A,01000000B  ;Set Acc for MOTOR ON,5",A.
E007  D385              OUT (85H),A     ;Configure FDCI chip

E009  3ED0    FDCRES:   LD A,11010000B  ;Load RESET command (D0H)
E00B  D380              OUT (80H),A     ;Command FDCI RESET
E00D  0600              LD B,0
E00F  10FE    DELAY:    DJNZ DELAY      ;Brief pause
E011  DB80              IN A,(80H)      ;Get drive status
E013  CB47              BIT 0,A         ;Test busy bit
E015  20F2              JR NZ,FDCRES    ;If busy force another reset

E017  3ED4    NREADY:   LD A,11010100B  ;Load INTERRUPT AT INDEX (0D4H)
E019  CD5EE0            CALL DISCOM     ;Command - wait for index
E01C  DB80              IN A,(80H)      ;Status after command complete
E01E  CB7F              BIT 7,A         ;Test for ready (STATUS BIT 7)
E020  20F5              JR NZ,NREADY    ;Loop if not ready

                        ;Seek track 0 on drive A
E022  3E0C    QAT00:    LD A,00001100B  ;Load RESTORE command (0CH)
E024  CD5EE0            CALL DISCOM     ;Command drive A to restore
E027  DB80              IN A,(80H)      ;Get drive status
E029  CB57              BIT 2,A         ;At track 0?
E02B  2000              JR NZ,BOOTGO    ;Yes. then jump on
                        ;JP ERROR  - Here if "FAILED TO RESTORE" -
                        ;goto recovery routine or report error.

                        ;Get ready to read data.
E02D  2100C0  BOOTGO:   LD HL,0C000H    ;Destination of 512 byte sector
E030  3E00              LD A,0          ;Load TRACK 0
E032   D381              OUT (81H),A     ;Set Track Register to 0
E034  3E01              LD A,1          ;Load SECTOR 1
E036  D382              OUT (82H),A     ;Set Sector Register to 1
```

```
E038  0E84           LD C,84H       ;Load C with DPOLL port number
E03A  3E8E           LD A,10001110B ;Load READ SECTOR command  (8EH)
E03C  D380           OUT (80H),A    ;Command a "Read Sector"

;Note:- Next code is very important.  The FDCI is designed
;       so that the Z80 flags reflect the conditions at the
;       DPOLL port.      7 6 5 4 3 2 1 0
;       The port is wired DRQ,0,0,0,0,0,0,INTRQ. So that
;       after IN D,(C) :-
; If port contents are zero then (NOT DRQ) "AND" (NOT INTRQ)
; If port contents are -ve then DRQ detected (Data Request)
; If port contents are +ve then INTRQ detected (Interrupt Request)

E03E  ED50   DRQ:    IN D,(C)  ;Get (DPOLL),DRQ,0,0,0,0,0,0,INTRQ
E040  CA3EE0         JP Z,DRQ  ;Loop as NOT DRQ "AND" NOT INTRQ
E043  DB83           IN A,(83H);either DRQ or INTRQ so read data
E045  77             LD (HL),A ;Store data
E046  23             INC HL    ;Next location
E047  FA3EE0         JP M,DRQ  ;If DRQ then not NOT INTRQ, so not...
                               ;..last data,loop back for next data.
                     ;Here because of INTRQ. I.e last byte received.
E04A  DB80           IN A,(80H)     ;Get drive status
E04C  E69D           AND 10011101B  ;Mask for bits required  (9DH)
E04E  2800           JR Z,GBOOT     ;Good read, so jump on & continue.
                     ;JP ERROR      "ERRORS" Perhaps retry

                ;Good boot..Move loader to 0080H
E050  2100C0 GBOOT:  LD HL,0C000H   ;512 byte sector starts
E053  118000         LD DE,80H      ;DE has Destination.
E056  018000         LD BC,128      ;CP/M loaders are only 128 bytes
E059  EDB0           LDIR           ;Transfer loader code to 80H
E05B  C38000         JP 80H         ;Jump into loader code.

                ;Discom, gives the command in Acc to the FDCI and
                ;waits for INTRQ to be returned = Command complete.
E05E  D380   DISCOM: OUT (80H),A    ;Send command in Acc to FDCI
E060  DB84   NINTRQ: IN A,(84H)     ;Poll for DRQ,0,0,0,0,0,0,INTRQ
E062  E601           AND 1          ;Looking for INTRQ only
E064  28FA           JR Z,NINTRQ    ;Branch if not INTRQ
E066  C9             RET            ;Exit if INTRQ as command done
```

THE END

The official INTERAK disk format is shown overleaf.

INTERAK OFFICIAL DISK FORMAT

Compiled by Bob Eldridge

Thanks are extended to Mr Wolf Schroeder for the design of this disk format.

Please use this format when initialising your disks. This will ensure that whilst different CP/M installations may be used the disks will be file compatable. I will foward a copy of the Interak format to the CPMUGUK for inclusion in their library as soon as possible.

This format is file compatable with W.Schroeders CP/M implimentation as stocked by Greenbank. (See Software library listing.)

Interak always uses double density.

For single sided 5.5" drives use this format with side set to 0.

For double sided 5.5" drives use this format with side set to 0 then repeat it on the other side with side set to 1.

3.5" disks are exactly the same as 5.5" for format and connection. This will allow users to stay with 5.5" for the time being, perhaps obtaining one 3.5" disk for program transfer at a later date.

To use the table issue a Write track command and pass the following bytes to the data regester at each DRQ.

Number of bytes (decimal)	Value of written byte (Hex)	
INDEX	(Initial pattern written at index pulse)	
32	4E	
12	00	
3	F6	Writes C2
1	FC	Index mark
32	4E	
SECTOR	(repeat the following 10 times changing sector number to suit the desired skew factor.)	
12	00	
3	F5	Writes A1
1	FE	ID address mark
1	__	Track number (0 through 4F) (0-79 decimal)
1	__	Side number (use 00 for side 0, and 01 for side 1)
1	__	Sector number (1 through 0A, (1-10 decimal)
1	02	Length of data, Interak DD is always 02
1	F7	Writes two CRC bytes
22	4E	
12	00	
3	F5	Writes A1
1	FB	Data address mark
512	E5	Data
1	F7	Writes two CRC bytes
32	4E	Sector trailer

Repeat from "SECTOR" 10 times and then continue writing 4E untill 2797 INTRQ is raised.

If you could inspect the disk after formating it, you would find :-

```
Index hole      4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
                00000000000000000000000000
                C2C2C2
Index mark      FC
                4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
Index end
Sector 1        00000000000000000000000000
                A1A1A1
ID addr mark    FE
Track number    05
Side number     00
Sector number   01
Data length     02
ID CRC          762A
                4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
                00000000000000000000000000
                A1A1A1
Data mark       FB
DATA (512)      E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
Data CRC        C40B
                4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
Sector 1 end
Sector 2        00000000000000000000000000
                A1A1A1
ID addr mark    FE
Track number    05
Side            00
Sector number   02
Length          02
ID CRC          2379
                4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
                00000000000000000000000000
                A1A1A1
Data mark       FB
Data (512)      E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
```

```
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
                E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5E5
Data CRC        C40B
                4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
Sector 2 end
Sector 3 as above
         end
Sector 4 as above
         end
Sector 5 as above
         end
Sector 6 as above
         end
Sector 7 as above
         end
Sector 8 as above
         end
Sector 9 as above
         end
Sector A as above
         end
All sectors ended. Pad out to index hole
Track trailer 4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
              4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
              4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E4E
Index hole    Track end
```

The number of track trailer 4E bytes written would vary with different disks but suffice it to say that the remaining space is padded out with 4E bytes until the 2797 raises INTRQ.

The example shown above has a skew factor of 1. Other skews simply involve different sequences of sector numbers. I.e

SKEW	SECTOR SEQUENCE	LOGIC OF CHOICE
0	1,1,1,1,1,1,1,1,1,1	As 1+0=1 silly example to show method.
1	1,2,3,4,5,6,7,8,9,A	As 1+1=2, 2+1=3 , 3+1=4 , 4+1=5 , 5+1=6 ,
2	1,3,5,7,9,2,4,6,8,A	As 1+2=3, 3+2=5 , 5+2=7 , 7+2=9 , 9+2=B=1=2,
3	1,4,7,A,3,6,9,2,5,8	As 1+3=4, 4+3=7 , 7+3=A , A+3=D=3 , 3+3=6 ,
4	1,5,9,3,7,2,6,A,4,8	As 1+4=5, 5+4=9 , 9+4=D=3, 3+4=7 , 7+4=B=1=2,
5	1,6,2,7,3,8,4,9,5,A	As 1+5=6, 6+5=B=1=2, 2+5=7 , 7+5=C=2=3, 3+5=8 ,
6	1,7,3,9,5,2,8,4,A,6	As 1+6=7, 7+6=D =3, 3+6=9 , 9+6=F=5 , 5+6=B=1=2,

As CP/M will search for the sector number in the ID field of the written disk, the order of the sectors on the disk does not matter. All disks will be readable by BIOS's with the TRANS word = 0 = No BIOS skew translation. Or if a BIOS translate table = 1,2,3,4,.....78,79,80 is used.

Apart from us all trying to use the same disk format we should also if possible use the same Disk Parameter Blocks. See CP/M Alteration guide page 26 and 27. Enclosed therefore is the Parameter Block for Double Sided Double Density 5.5" disks as used on the the Interak computer.

INTERAK 5.5" DOUBLE SIDED DOUBLE DENSITY DISK PARAMETER BLOCK

NOTES: 16 bit values are shown low byte first as in the Z80 standard.

HEX VALUE IN BIOS	DECIMAL VALUE		DESCRIPTION
5000	80	SPT	Sectors Per Track (Logical 128 byte sectors, real=20)
05	5	BSH	Block Shift Factor
1F	31	BLM	BLM=31 & BSH=5 produce BLS=4096 see CP/M manual p27
03	3	EXM	EXtent Mask. (DSM<256) & BLS = 4096 then EXM = 3
C200	194	DSM	Disk Size Modulus. (DSM+1)*BLS= Total disk storage.
FF00	255	DRM	Number of directory entries -1
C0	192	AL0	AL0 AL1 = Reserved storage for directory entries. I.e
00	0	AL1	reserve 2 4096 byte blocks for 256 32 byte entries.
1000	16	CKS	Directory check vector (Checked directory entries.)
0200	2	OFF	Reserved tracks for operating system (CP/M)

The derevations of the above table can be understood by considering the following sequence of calculations :-

First we choose a data BLock Size (BLS) as 4096 then :-

SPT=80 as 20 * 512 byte real sectors produce 80 * 128 byte CP/M logical sectors.

DSM=194 as :-

```
Disk total capacity (DTOTAL)     = (80 tracks)*(20 sectors)*(512 bytes)
                                 = 819200 bytes
Disk operating system (DSYSTEM)  = ( 2 tracks)*(20 sectors)*(512 bytes)
                                 =  20480 bytes
Disk data storage space (DDATA)  = DTOTAL-DSYSTEM
                                 = 819200-20480
                                 = 798720 bytes
Remembering our Block size (BLS)= 4096
Gives DSM (Disk Size Modulus)    = INT(DDATA/BLS)-1)
                                 = INT((798720/4096)-1)
                                 = INT(195-1)
                             DSM = 194
```

BSH=5 because BLS=4096

BLM=31 because BLS=4096

EXM=3 as BLS=4096 and DSM is less than 256.

DRM=255. This is chosen to give 256 directory entries per disk.

OFF=2 as CP/M is given the first two tracks on the disk to live on. This means that the first real track for data storage in track 2.

CKS=16. This is slightly naughty as it should be (DRM+1)/4=64. It will work but gives reduced protection against accidental overwriting of changed disks.

AL0,AL1. These work together to produce a reserved directory space on track 2 of the disk. Consider our needs of 256 directory entries each 32 bytes long. This gives a directory storage requirment of 8192 bytes. A block or BLS=4096 bytes, so we need 2 BLS or 2 blocks. AL0,AL1 together are 1100 0000 0000 0000, each set bit reserving one block so a value of C000 reserves two blocks of 4096 bytes for the on disk directory.

If you have coded your tables correctly the above, after the command ..

```
A>STAT DSK:

  A: Drive Characteristics
6240: 128 Byte Record Capacity
 780: Kilobyte Drive Capacity
 256: 32 Byte Directory Entries
  64: Checked Directory Entries
 512: Records/ Extent
  32: Records/ Block
  80: Sectors/ Track
   2: Reserved Tracks
```

should appear on the screen.

I will publish parameter blocks for the other types of drives as soon as I can get hold of them.

By all means construct your own BIOS and system but please try to retain compatability with other users by using the same format and parameter areas.

By the way if you would like to see what your CP/M serial number is then find the start address of your CCP and look at CCP+328H for one copy. To check that you are correct compare it with the other copy at CCP+800H. Another check that you are looking in the right place is to step back from CCP+328H and you should find the CP/M command table holding the ASCII string:-

DIRERATYPESAVERENUSER

For example in the INTERAK system, Boot up with B. Type CPMMAP and read the value called CCP FWA. If you have Wolf's 20K system then the CCP FWA will be 2E00H. Therefore :-

2E00H+328H = 3128H First copy, immediatly below the above string.
and 2E00H+800H = 3600H Second copy.

Now press reset to get back to Wolf's monitor and use MD 3128 312F for the first copy and MD 3600 3608 for the second copy. The numbers are six bytes long and both are checked for equality before CP/M will function correctly.

Bob Eldridge.

LETTERS

Please write with comments, ideas, complaints and suggestions. Name and address must be enclosed, but can be with-held. Responsibility for views and comments expressed cannot be held by the editor as members letters are published with the minimum changes (deleted bad language etc). (Note; I type what I see, if you forget a word then it will be missing in the newsletter, also if you spell a word wrong then it's quite likely that I will punch it in wrong.)

Dear Mr Eldridge,

This may be regarded as somthing of a 'parting shot' between me and 'Interaktion'!!. I see from the last issue that subs are now due, but I shall not be renewing mine this year. You may well already be aware of the reason for my disenchantment, and this is why I have written to you, since I am far from convinced that said Mr Vella has not retired to the Bahamas on the proceeds of Interaktion subs and payments for software, never received!.

I would be the first to aknowledge that it is all a voluntary business, but I mustn't be the first to have sent money, and several reminders for software, and received only a deathly silence in return; When money is involved I feel that there is then a duty to 'deliver the goods' and one cannot hide behind such a flimsy excuse.

I have spoken to David Parkins at Greenbank, but I get the impression that he is simply embarrassed and does'nt know what to do. Again, I feel that if they are prepared to put in their name behind Interaktion they should make more positive attempts to make something happen!

Also, I would guess that I am not the first to offer help in this direction, and if you wish to take up this offer then I have certain skills and access to facilities which could be of some help - just let me know.

I look foward to hearing from you in due course.

M. WARTON, 8 OVITTS CLOSE, WINSLOW, BUCKS, MK18 3QD.

[ED - I have spoken to Mike on the telephone regarding the sorry state of affairs he describes. We are aware that things are not as they sould be. Pete Vella is obviously overloaded and we have taken action to reduce his load. From now on Tom Evans will be controlling the subs and each individual software author will supply and support his own product. (The two items that were given to us anonimosly will be supplied by me). Hopefully this will improve the services. Speaking for David, (If I may), Greenbank print and distribute the newsletter but they have no control over its contents or over the activities of the group. David could not really help, and was probally expressing distress at the customer disatisfaction. PETE please process Mikes order for Veltext.]

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Richard Bowyer

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